What is claimed is:

1. A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit.

2. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

wherein the second load comprises a fourth control device;

wherein the node of the second load is a signal input of the fourth control device; and

wherein the first load is a fifth control device, a control input of the fourth control device is coupled to a control input of the fifth control device, and a control input of the third control device is coupled to the output.

3. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

a fourth control device including a control input and a controlled signal output;

wherein the second load comprises a fifth control device;

wherein the node of the second load is a signal input of the fifth control device; and

wherein the first load is a sixth control device, the control input of the fourth control device is coupled to a control input of the sixth control device, a control input of the third control device is coupled to the output, and a the controlled signal output of the fourth control device is coupled to the controlled signal output of the first control device.

4. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

a fourth control device including a control input and a controlled signal output;

wherein the second load comprises a fifth control device;

wherein the node of the second load is a signal input of the fifth control device; and

wherein the first load is a sixth control device, the control input of the fourth control device is coupled to a control input of the sixth control device, a control input of the third control device is coupled to a controlled signal output of the third control device, and the controlled signal output of the fourth control device is coupled to the controlled signal output of the first control device.

5. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first transistor including a source and a well both connected to a first voltage, the first transistor including a gate and a drain;

a second transistor including a source and a well both connected to the first voltage, the second transistor including a gate and a drain, wherein the second transistor gate is connected to the first transistor gate and a second voltage;

a third transistor including a source and a well both connected to the first voltage, the third transistor including a gate and a drain both connected to the output;

a fourth transistor including a source connected to the second voltage, a gate connected to the input, and a drain connected the first transistor drain; and

a fifth transistor including a source connected to the input, a gate connected to the fourth transistor drain, and a drain connected to the output.

6. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first transistor including a source and a well both connected to a first voltage, the first transistor including a gate and a drain;

a second transistor including a source and a well both connected to the first voltage, the second transistor including a gate and a drain, wherein the second transistor gate is connected to the first transistor gate and a second voltage; and

a feedback biasing circuit, wherein the feedback biasing circuit consists of:

a third transistor including a source and a well both connected to the first voltage, the third transistor including a gate and a drain both connected to the output;

a fourth transistor including a source connected to the second voltage, a gate connected to the input, and a drain connected the first transistor drain; and

a fifth transistor including a source connected to the input, a gate connected to the fourth transistor drain, and a drain connected to the output.

7. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

quick-charging means for simultaneously raising potentials of a bit line and the output;

a load for a memory device being sensed, and

a feedback means for preventing the potential of the bit line from exceeding a read-bias potential.

8. The system of claim 1, wherein at least one of the first circuit and the second circuit include:

an input;

an output;

quick-charging means for simultaneously raising potentials of a bit line and the output and for continuing to raise the potential of the output when the potential of the bit line is no longer raised;

a load for a memory device being sensed, and

a feedback means for preventing the potential of the bit line from exceeding a read-bias potential.